Exponential-gap fanin-hierarchy for border depth-3 circuits

Joint work with Nitin Saxena (IIT Kanpur).

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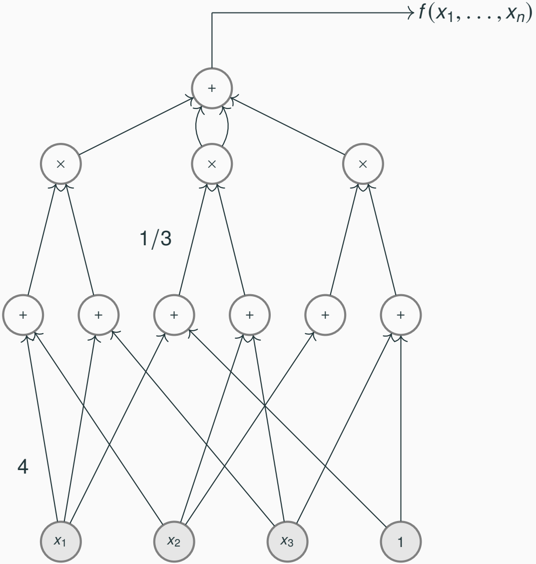
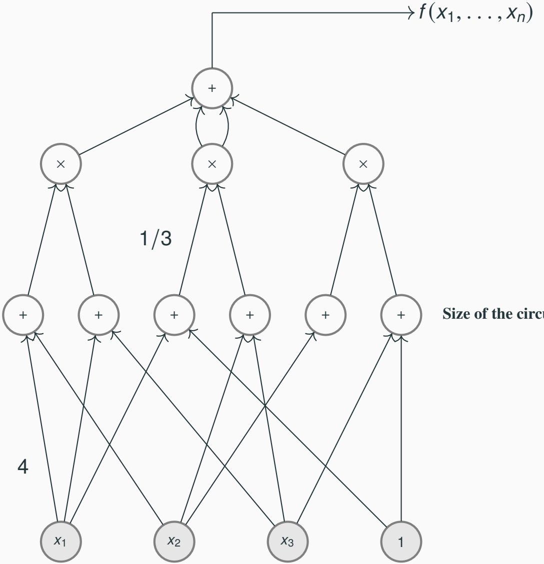
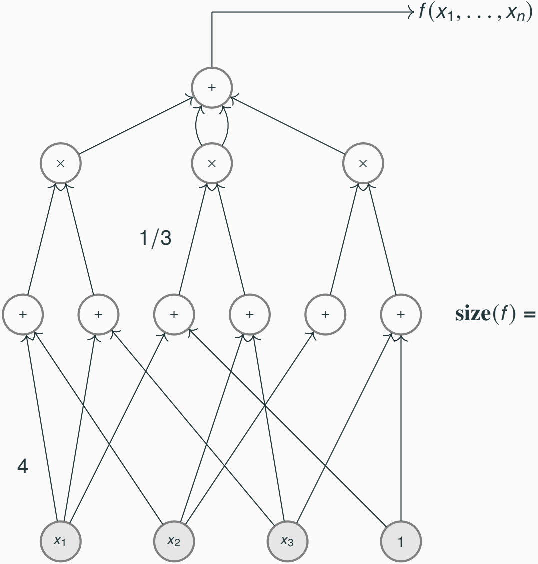


Algebraic circuits



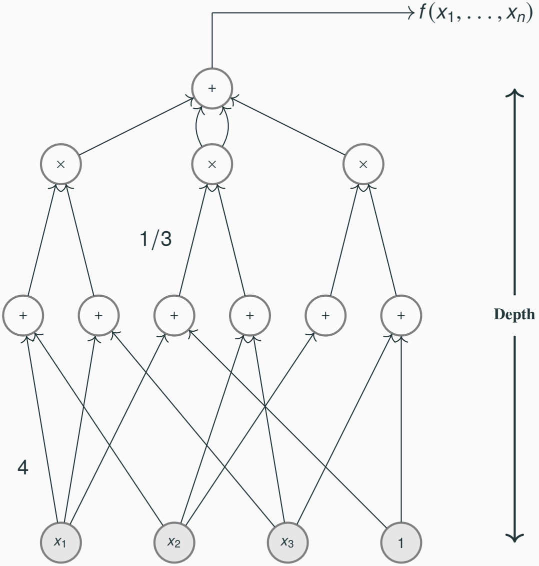
Size of the circuit = number of nodes + edges

Algebraic circuits



size(f) = min size of the circuit computing f

Algebraic circuits



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- VBP: The class VBP is defined as the set of all sequences of polynomials $(f_n)_n$ with polynomially bounded $\mathrm{dc}(f_n)$.

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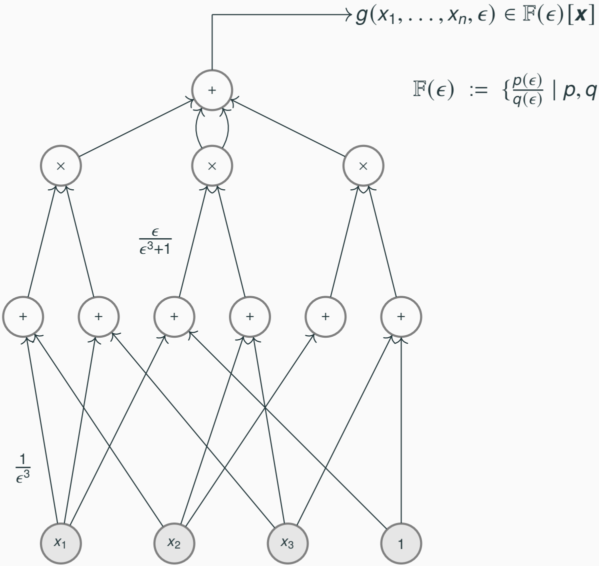
- We will work with *'approximative circuits'*.

Approximative circuits



$$\mathbb{F}(\epsilon) := \{\tfrac{p(\epsilon)}{q(\epsilon)} \mid p, q \in \mathbb{F}[\epsilon], q(\epsilon) \neq 0\}$$

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- Suppose, we assume the following:
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- Summary: g_0 is really something **non-trivial** and being 'approximated' by the circuit since $\lim_{\epsilon \to 0} g(\boldsymbol{x}, \epsilon) = g_0$.

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- When ℓ_i are non-homogeneous, we will write this as $h \in \overline{\Sigma^{[s]} \wedge \Sigma}$.
- $\overline{\mathsf{WR}}(x^{d-1}y) = 2$, since, $d \cdot x^{d-1}y + O(\epsilon) = (x + \epsilon y)^d - x^d$.

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  - What about border depth-3 circuits?

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- The same holds if we replace by $\det_n$.

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- So, $\Sigma^{[k]}\Pi\Sigma \subsetneq \mathsf{VBP}$!

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- det_n *cannot* be computed by a $\Sigma^{[k]}\Pi\Sigma$-circuit, *regardless* of the product fan-in.

  Proof sketch: Let $\sum_{i\in[k]} T_i = \mathsf{det}_n$, where $T_i \in \Pi\Sigma$, product of linear polynomials.

  - Pick ℓ_1 from T_1 and consider $\mathcal{I}_1 := \langle \ell_1 \rangle$.
  - LHS $\mod \mathcal{I}_1$, becomes $\sum_{i\in[k-1]} T_i'$ while $\mathsf{det}_n \mod \mathcal{I}_1 \neq 0$.
  - Keep repeating and each time include an independent ℓ_i in the ideal $\mathcal{I}_i$.
  - At the end, there is some $\mathcal{I}_k$ such that RHS has become 0 while LHS is *non-zero* (because $k << n$).

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- How about $\overline{\Sigma^{[k]}\Pi\Sigma}$?

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Border depth-3 fan-in 2 circuits are 'universal' [Kumar 2020]

Let P be *any* n-variate degree d polynomial. Then, $P \in \overline{\Sigma^{[2]}\Pi^{[D]}\Sigma}$, where $D := \exp(n, d)$.

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Border of polynomial-sized depth-3 top-fanin-2 circuits are 'easy' [Dutta-Dwivedi-Saxena FOCS 2021].

$\overline{\Sigma^{[2]}\Pi\Sigma} \subseteq \mathsf{VBP}$, for polynomial-sized $\overline{\Sigma^{[2]}\Pi\Sigma}$-circuits. In particular, any polynomial in the border of top-fanin-2 size-s depth-3 circuits, can also be exactly computed by a linear projection of a $\mathsf{poly}(s) \times \mathsf{poly}(s)$ determinant.

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Remark. The result holds if one replaces the top-fanin-2 by arbitrary constant k.

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  - Since, $\mathsf{IMM}_{n,d} \in \mathsf{VBP}$, $\overline{\Sigma^{[k]}\Pi\Sigma} \neq \mathsf{VBP}$.

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- What does work (if at all!)?

Hierarchy theorem

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- Classical is about *impossibility* while in border, it is about *optimality*.

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- *Infinitely* many factorizations may give *infinitely* many limits.

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- The worst case:

$$f + \epsilon S \;=\; T_1 + T_2\,,$$

where T_i has each linear factor of the form $1 + \epsilon\ell$!

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- So, all-non-homogeneous is all we have to care!
- For $k > 2$, we need a technical lemma, but still can be reduced!

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- Thus, $s \geq 2^{\Omega(d)}$!

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- Shifting is problematic for showing lower bound!
- So, the current proof is about pre-processing (technical lemma, reducing to all-non-homogeneous) & DiDIL.

Proof sketch for $k = 2$

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$$
\begin{aligned}
P_d + \epsilon \cdot S =\; & T_1 + T_2 \\
\implies \Phi(P_d) + \epsilon \cdot \Phi(S) =\; & \Phi(T_1) + \Phi(T_2) \\
\implies \Phi(P_d)/\tilde{T}_2 + \epsilon \cdot \Phi(S)/\tilde{T}_2 =\; & \epsilon^{a_2} + \Phi(T_1)/\tilde{T}_2 \\
\implies \partial_z\left(\Phi(P_d)/\tilde{T}_2\right) + \epsilon \cdot \partial_z\left(\Phi(S)/\tilde{T}_2\right) =\; & \partial_z\left(\Phi(T_1)/\tilde{T}_2\right) =: g_1 \;. \qquad (1)
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$$\begin{aligned} P_d + \epsilon \cdot S &= T_1 + T_2 \\ \implies \Phi(P_d) + \epsilon \cdot \Phi(S) &= \Phi(T_1) + \Phi(T_2) \\ \implies \Phi(P_d)/\tilde{T}_2 + \epsilon \cdot \Phi(S)/\tilde{T}_2 &= \epsilon^{a_2} + \Phi(T_1)/\tilde{T}_2 \\ \implies \partial_z \left(\Phi(P_d)/\tilde{T}_2\right) + \epsilon \cdot \partial_z \left(\Phi(S)/\tilde{T}_2\right) &= \partial_z \left(\Phi(T_1)/\tilde{T}_2\right) =: g_1 \,. \end{aligned} \tag{1}$$

- $\lim_{\epsilon \to 0} g_1 = 1/t_2 \cdot \partial_z(\Phi(P_d))$, where $\mathbb{F} \ni t_2 := \lim_{\epsilon \to 0} \tilde{T}_2$, because $\lim_{\epsilon \to 0} \prod(1 + \epsilon \ell_i) = 1$.

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- Here Σ means just a linear polynomial ℓ.

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- $\deg(P_d) = d \implies \deg_z(\Phi(f)) = d \implies \deg_z(\partial_z(\Phi(P_d))) = d - 1$.

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- $\deg(P_d) = d \implies \deg_z(\Phi(f)) = d \implies \deg_z(\partial_z(\Phi(P_d))) = d - 1$.
- Suffices to compute $\lim_{\epsilon \to 0} g_1 \mod z^d$.

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Thus,

$$\begin{aligned}\lim_{\epsilon \to 0} g_1 \mod z^d &\equiv \lim_{\epsilon \to 0} (\Pi\Sigma/\Pi\Sigma) \cdot \left(\sum \mathsf{dlog}(\Sigma)\right) \mod z^d \\ &\equiv \lim_{\epsilon \to 0} (\Pi\Sigma/\Pi\Sigma) \cdot (\Sigma \wedge \Sigma) \mod z^d \\ &\in \overline{(\Pi\Sigma/\Pi\Sigma) \cdot (\Sigma \wedge \Sigma)} \mod z^d \,.\end{aligned}$$

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- The above is because $\lim_{\epsilon \to 0} \prod (1 + \epsilon \ell) = 1$.
- Thus, $1/t_2 \cdot \partial_z(\Phi(P_d)) = \lim_{\epsilon \to 0} g_1 \in \overline{\Sigma \wedge \Sigma}$.
- Thus, $\Phi(P_d) \in \overline{\Sigma \wedge \Sigma} \implies P_d \in \overline{\Sigma \wedge \Sigma}$.

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- Can we extend the hierarchy theorem to bounded (top & bottom fanin) depth-4 circuits? i.e., for a *fixed* constant δ, is $\overline{\Sigma^{[1]}\Pi\Sigma\Pi^{[\delta]}} \subsetneq \overline{\Sigma^{[2]}\Pi\Sigma\Pi^{[\delta]}} \subsetneq \overline{\Sigma^{[3]}\Pi\Sigma\Pi^{[\delta]}} \ldots$, where the respective gaps are exponential? Clearly, $\delta = 1$ holds, from this work.

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Thank you! Questions?